OTI-068 DATABOOK

April 28, 1993

Preface

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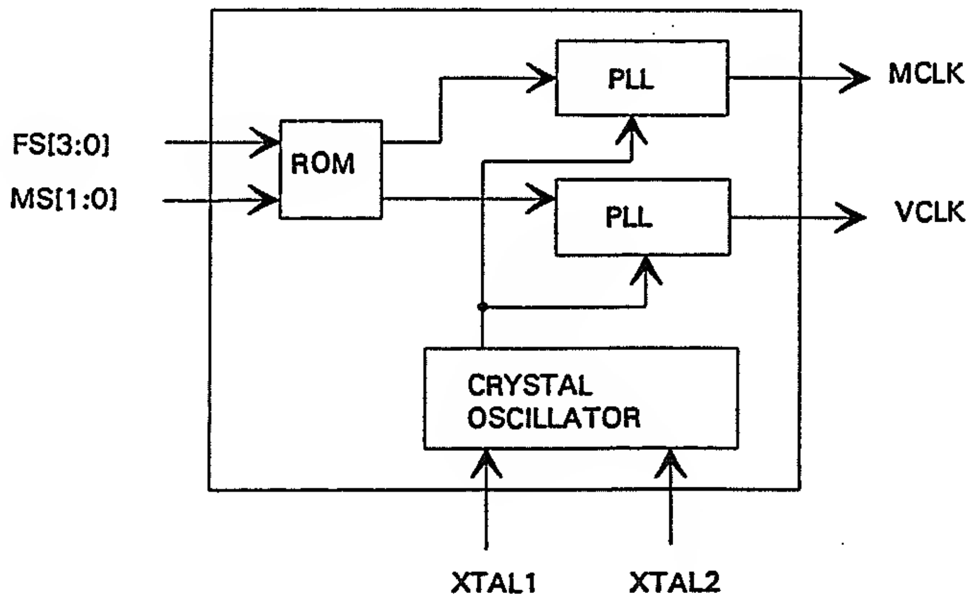
DESCRIPTION

The OTI-068 is a Dual Clock Synthesizer ideal for use with high performance video display systems. It is capable of generating 16 video pixel clock frequencies and 4 memory clock frequencies for use with EGA, VGA and Super VGA systems. The PLL's have an internal loop filter which reduces component count on the board. The PLL design permits clean transitions between clock frequencies.

FEATURES

- Single +5V supply
- Sixteen Video Clock and 4 Memory Clock frequencies
- Integrated loop filter
- Advanced PLL design for low phase-jitter
- 80 MHz maximum output frequency
- Supports VGA, Super VGA, XGA, 8514A, EGA, CGA MCGA and MDA.
- Supports high refresh VESA rates with the OTI-077 and OTI-087 VGA controllers.
- Low power CMOS design

FUNCTION BLOCK DIAGRAM



APPLICATIONS

Layout Considerations

Although designing a video graphics adapter card or motherboard video is relatively straight-forward, it requires precautions in board layout if jitter-free performance is to be realized.

1) Do not share grounds with components not related to the OTI-068.
2) Connect Vss directly to the ground plane if available.
3) Separate all analog and digital Vss and Vdd connections for VCLK operation at or above 78 MHz.
4) Always connect all Vss and Vdd pins.

Frequency Reference

The internal reference oscillator contains all of the passive components required. An appropriate parallel resonant crystal should be connected between XTAL1 and XTAL2. Oak Technology applications have a 14.31818 MHz crystal between XTAL1 and XTAL2. Maintain short lead lengths between the crystal and the OTI-068. In some application it may be desirable to utilize the bus clock. If the signal amplitude is equal to or greater than 3.5 volts, it may be connected directly to XTAL1. If the signal amplitude is less than 3.5 volts, connect the clock through a 0.047 microfarad capacitor to XTAL1. Keep the lead length of the capacitor to XTAL1 to a minimum to reduce noise susceptibility. This input is internally biased at Vdd/2 since TTL compatible clocks typically exhibit a Voh of 3.5 V. Capacitively coupling the input increases noise immunity. The OTI-068 is not sensitive to the duty cycle of the bus clock; however, the quality of this signal varies considerably with different motherboard designs. As the quality of this signal is typically outside of the control of the graphics adapter card manufacturer, it is suggested that this signal be buffered on the graphics adapter board. XTAL2 should be left open in this configuration.

Output Circuit Considerations

As the dot clock is usually the highest frequency present in a video system, consideration should be given to EMI. To minimize EMI problems, the trace which connects VCLK or MCLK and other components in the system should be kept as short as possible. The OTI-068 outputs have been designed to minimize overshoot. In addition, it may be helpful to place a ferrite bead in these signal paths to limit the propagation of high order harmonics of this signal. A suitable device would be a Ferroxcube 56-590-65/4B or equivalent. This device should be placed physically close to the OTI-068. A 33 to 47 Ohm series resistor in this path may be necessary to reduce ringing and reflection of the signal and may reduce phase jitter as well as EMI.

Digital Inputs

FS0, FS1, FS2, FS3 are the TTL compatible frequency select inputs for the binary code corresponding to the desired frequency. The internal power-on clear signal will force an initial frequency code corresponding to an all zero input state. MS0 and MS1 are the corresponding memory select inputs and are not strobed.

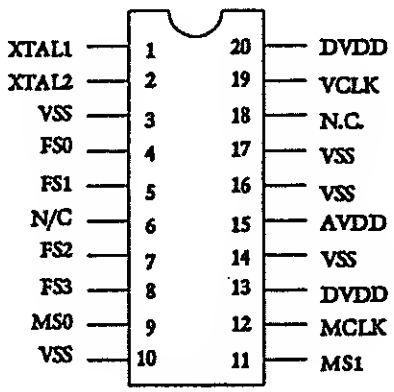
AC Timing Characteristics (Output Clock): TA= 0°C to 70°C, Vdd=5V+/-10%, Vss=0V

Symbol	Parameter	Min	Max	Notes
Tr	Rise Time	-	3 ns	Duty Cycle 40% Min
Tf	Fall Time	-	3 ns	60% Max
-	Frequency Error	-	0.5 %	
Fmax	Maximum Frequency	-	80 MHz	

The following notes apply to all parameters presented in this section.

1. XTAL Frequency = 14.31818 MHz.
2. Rise and fall time between 0.8 and 2.0 VDC.
3. Output pin loading = 25pF
3. Duty cycle measure at 1.4V

PIN DIAGRAM



OTI-068 STANDARD FREQUENCIES

The OTI-068 uses the FS[2:0] and MS[1:0] to determine which frequencies will be used. The table below shows the various VCLK and MCLK frequencies. CSEL[2:0] pins of the VGA controller controls the FS[2:0] pins of the OTI-068. A jumper or switch controls FS3. MS[1:0] is typical controlled by a jumper or switch. MS[1:0] can also be driven by an external signal or hardwired.

Oak Standard Pixel Clock Table					
FS3	FS2	FS1	FS0	Video Clock Address (HEX)	Frequency (MHz)
0	0	0	0	0	25.175
0	0	0	1	1	28.322
0	0	1	0	2	65.000
0	0	1	1	3	44.900
0	1	0	0	4	28.322
0	1	0	1	5	36.000
0	1	1	0	6	40.000
0	1	1	1	7	36.000

High Vertical Refresh Table					
FS3	FS2	FS1	FS0	Video Clock Address (HEX)	Frequency (MHz)
1	0	0	0	8	25.175
1	0	0	1	9	28.322
1	0	1	0	A	78.000
1	0	1	1	B	65.000
1	1	0	0	C	63.000
1	1	0	1	D	72.000
1	1	1	0	E	40.000
1	1	1	1	F	50.000

Memory Clock Table			
MS1	MS0	Memory Clock Address (HEX)	Frequency (MHz)
0	0	0	44.000
0	1	1	50.000
1	0	2	66.000
1	1	3	40.000

All patterns shown above use 14.31818 MHz as the input reference frequency.